EE 508
Lecture 29

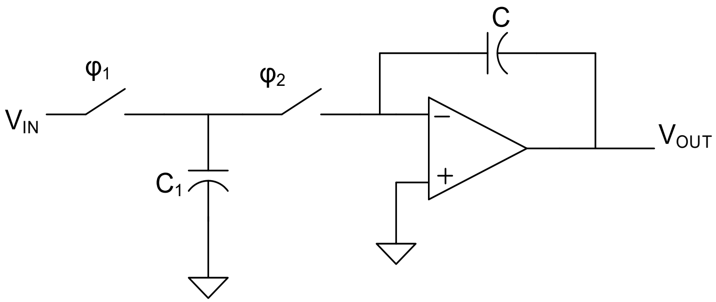
Nonideal Effects in Switched Capacitor Circuits

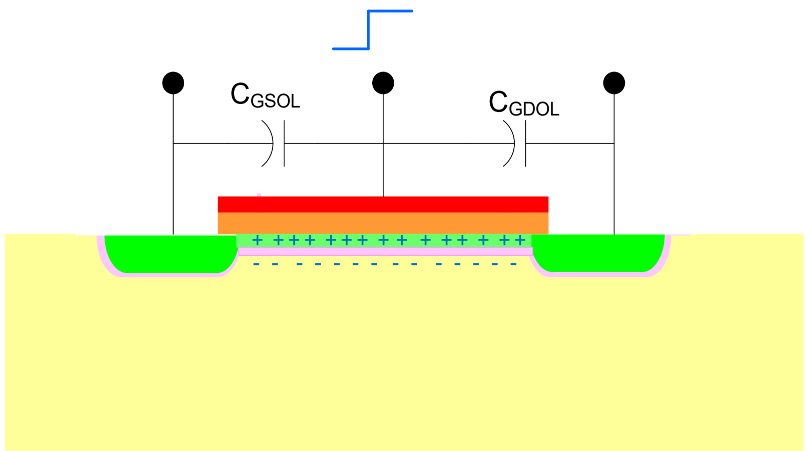
Noise

Switched-Resistor Filters

Other Integrators

Charge Injection

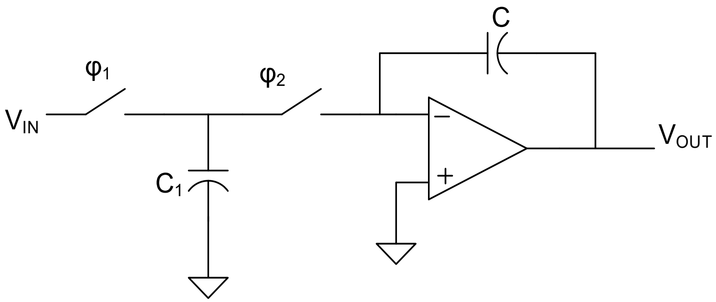


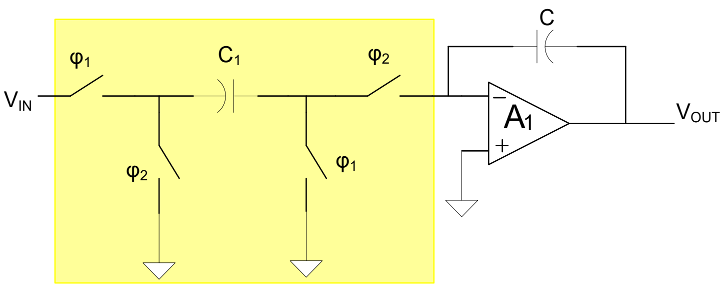


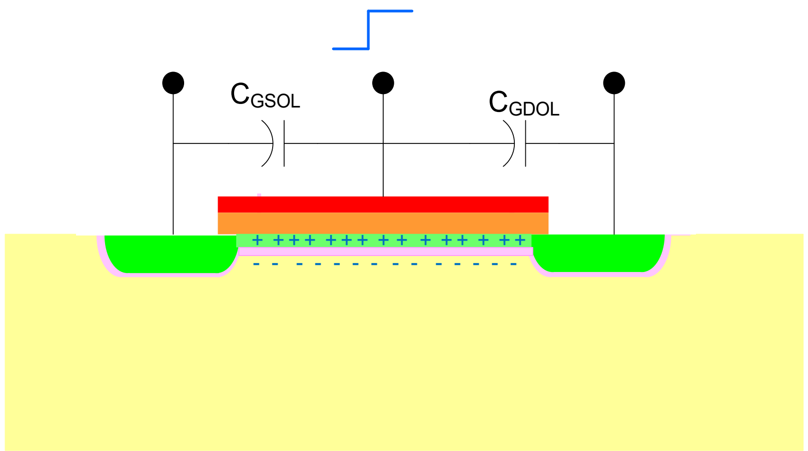
n-channel MOSFET

- If Φ_1 opens slowly, channel charge will all exit through V_{IN}
- If Φ_1 opens quickly, some charge will exit to left and some to right and split depends upon impedances seen to left and right
- Often not practical to open switches slowly
- Channel charge injection introduces errors in charge transfer and affects linearity

Charge Injection



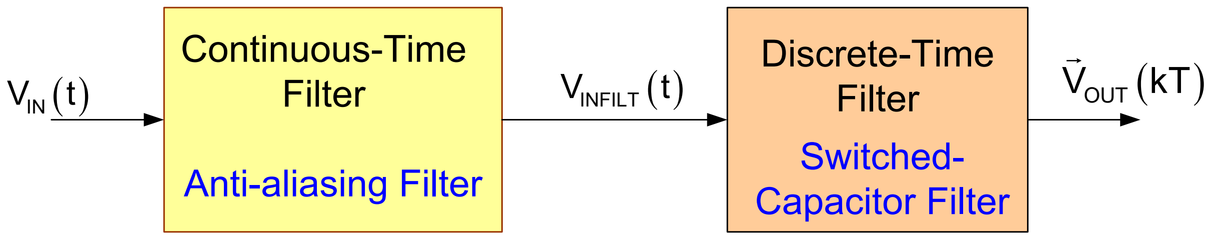


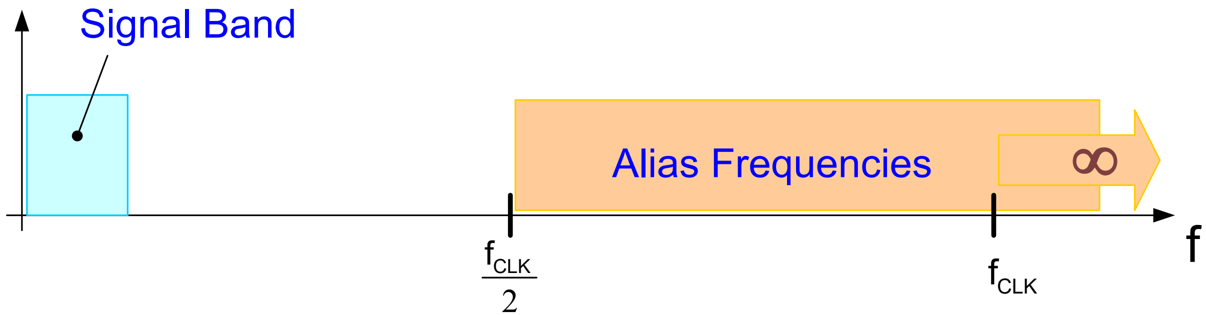


n-channel MOSFET

- Somewhat more complicated in multi-switch implementations
- There will naturally be a small amount of skew on clocks and this skew will affect charge injection
- Charge injection from some switches can be reduced or eliminated by using advanced clock (e.g. lower Φ_1 switch opens before upper Φ_1 switch)

Anti-aliasing filter often required to limit frequency content at input to SC filters





Why not just make the clock frequency >> signal band edge ?

Recall in the continuous-time RC-SC counterparts

$$f_{POLES} \cong \frac{1}{RC} \cong f_{CLK} \, C_1 / C$$

Since f_{POLES} will be in the signal band (that is why we are building a filter) large f_{CLK} will require large capacitor ratios if $f_{CLK} >> f_{POLES}$

- Large capacitor ratios not attractive on silicon (area and matching issues)
- High f_{CLK} creates need for high GB in the op amps (area,power, and noise increase)

Often f_{CLK}/f_{POLES} in the 10:1 range proves useful (20:1 to 5:1 typical)

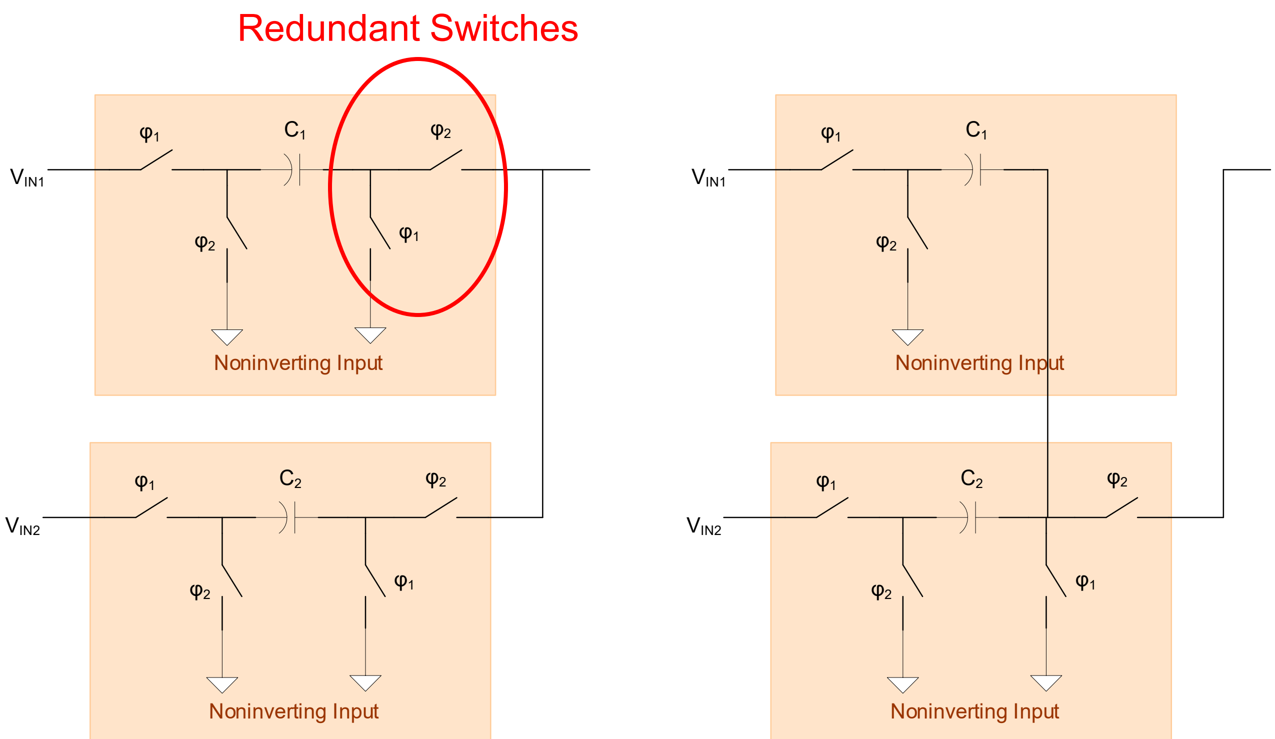
Review from Last Lecture

Nonideal Effects in Switched Capacitor Circuits

- Parasitic Capacitances
- Charge Injection
- Aliasing
- Redundant Switch Removal
- Matching
- Noise

Review from Last Lecture

Elimination of Redundant Switches



Switched-Capacitor Input with Redundant Switches

Switched-Capacitor Input with Redundant Switches Removed

Although developed from the concept of SC-resistor equivalence, SC circuits often have no Resistor-Capacitor equivalents

Review from Last Lecture

Nonideal Effects in Switched Capacitor Circuits

- Parasitic Capacitances
- Charge Injection
- Aliasing
- Redundant Switch Removal
- Matching
- Noise

Review from Last Lecture

Matching

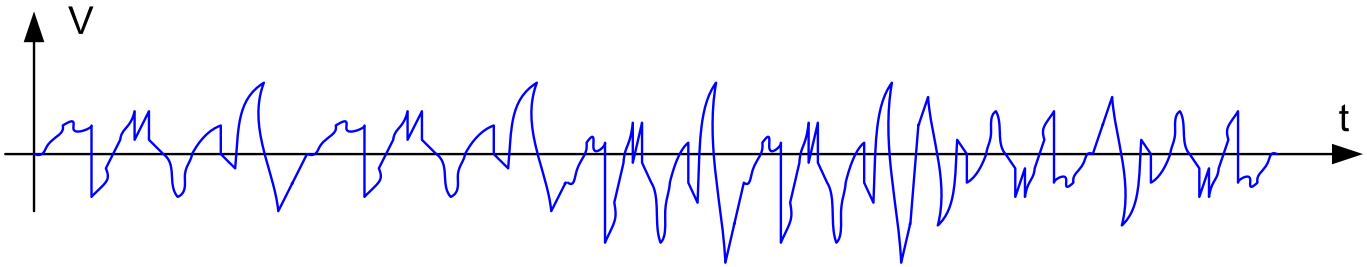
- Matching is a statistical concept and directly relates to yield
- With good layout, matching to 0.01% or better can be achieved
- Common-centroid widely used to eliminate gradient effects
- Pelgrom parameter useful for analytically predicting yield with common-centroid layouts
- Area affects local variations
- Little in the literature or in PDKs to predict matching without gradient cancellation
- Must match all contacts and interconnects to get good matching
- Neighbor effects are important

Review from Last Lecture

Nonideal Effects in Switched Capacitor Circuits

- Parasitic Capacitances
- Op Amp Affects
- Charge Injection
- Aliasing
- Redundant Switch Removal
- Matching
- Noise

Noise in Continuous-time Linear Systems



Noise in continuous-time systems

$$v_{RMS} = \sqrt{\lim_{T_x \to \infty}\left(\frac{1}{T_X}\int_0^{T_x} v_n^2(t)dt\right)}$$

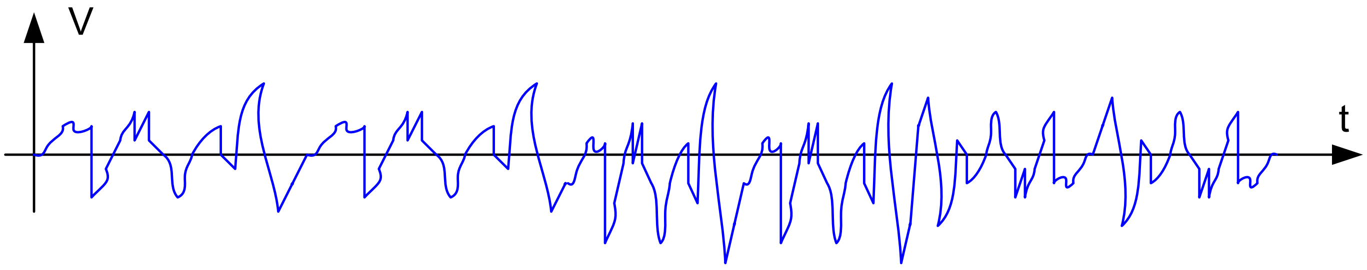
$\int_0^{T_x} v_n^2(t)dt$ is a random variable

At the design phase, we do not know what the time-domain noise characteristics will be

$$v_{RMS} = E\left(\sqrt{\lim_{T \to \infty}\left(\frac{1}{T}\int_0^{T} V^2(t)dt\right)}\right)$$

E denotes the expected value of the random variable

Noise in Continuous-Time Linear Systems



Noise often characterized by the spectral density S

$$\mathcal{v}_{RMS} = \sqrt{\left(\int_0^\infty S(f)df \right)}$$

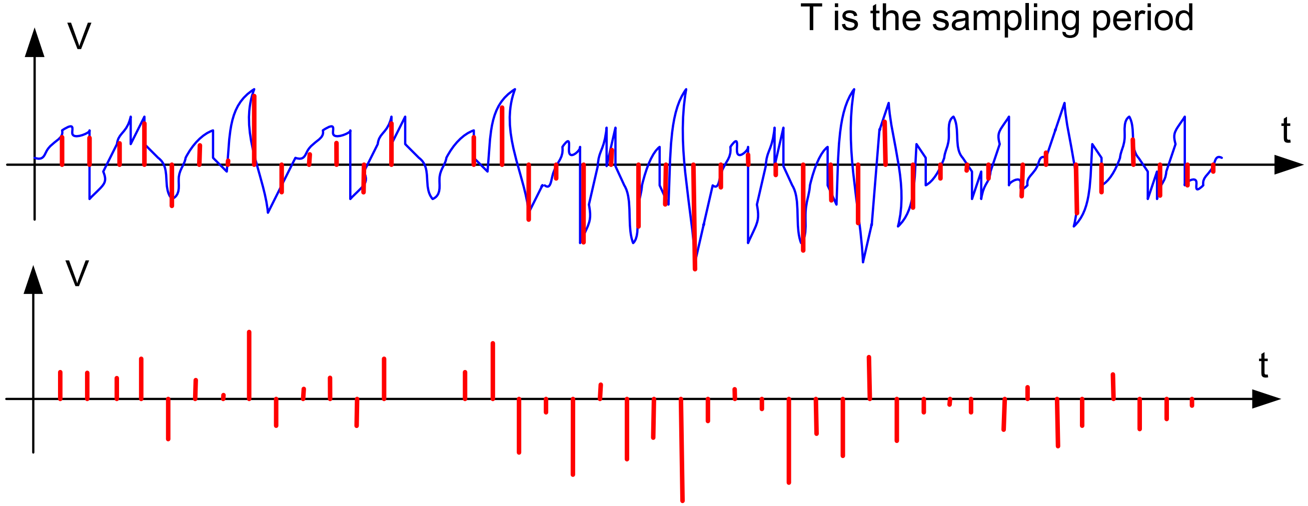
$$\int_{f=0}^{\infty} S(f)df = \lim_{f_x \to \infty} \int_{f=0}^{f_x} S(f)df$$

Thus

$$\sqrt{\lim_{T_x \to \infty} \left(\frac{1}{T_X} \int_0^{T_x} \mathcal{v}_n^2(t)dt \right)} = \sqrt{\left(\int_0^\infty S(f)df \right)} = \sqrt{\lim_{f_x \to \infty} \int_{f=0}^{f_x} S(f)df}$$

Relation between continuous-time and discrete-time noise

Assume $v_n(t)$ is a continuous-time noise source
T is the sampling period



Noise in discrete-time linear systems

$$\vec{V}(kT) = \left\langle v_n(mT) \right\rangle_{m=0}^{\infty}$$

$$\vec{V}_{RMS} = \sqrt{\lim_{M\to\infty}\left(\frac{1}{M}\sum_{k=0}^{M} v_n^2(kT)\right)}$$

$$\sigma\left(v_n(kT)\right) = v_{RMS}$$

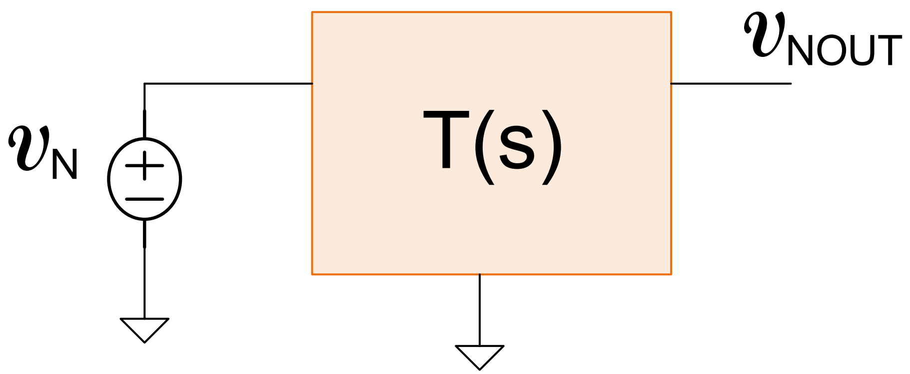
Noise in continuous-time linear systems

$$v_{RMS} = E\left(\sqrt{\lim_{T\to\infty}\left(\frac{1}{T}\int_0^T V^2(t)dt\right)}\right)$$

Noise in discrete-time system is identical to that of the continuous-time system from which it was sampled

$$\vec{V}_{RMS} = v_{RMS}$$

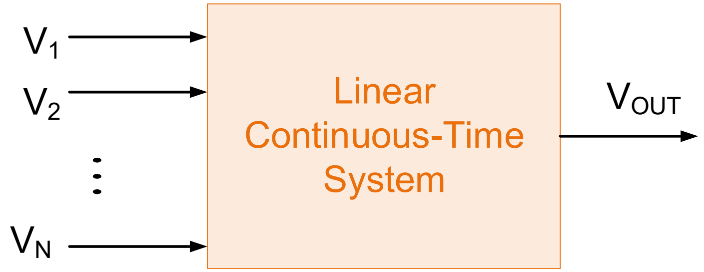
Noise review in Linear Systems (Filters)



Component of spectral density at output due to any noise source with spectral density S_X given by

$$S(\omega) = S_X \left|T(j\omega)\right|^2$$

Noise Summing in continuous-time Linear Systems



$$V_{OUT}(s) = \sum_{i=1}^{N} T_i(s) V_i(s)$$

If $V_1, V_2, \ldots V_N$ are noise sources in a Linear Continuous-Time System with spectral densities S_1, S_2, $\ldots S_N$, then

$$S_{OUT} = \sum_{i=1}^{N} S_i \bullet \left|T_i(j\omega)\right|^2$$

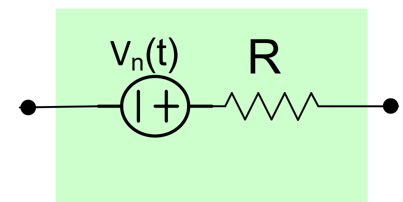
$$\mathcal{V}_{OUT\_RMS} = \sqrt{\int_{f=0}^{\infty} S_{OUT} df} = \sqrt{\int_{f=0}^{\infty} \sum_{i=1}^{N} S_i \bullet \left|T_i(j\omega)\right|^2 df}$$

Noise

- Capacitors do not contribute any noise

- Resistors contribute thermal noise

- Switches contribute thermal noise



Noise model of any resistor
$V_n(t)$ dependent on value of R

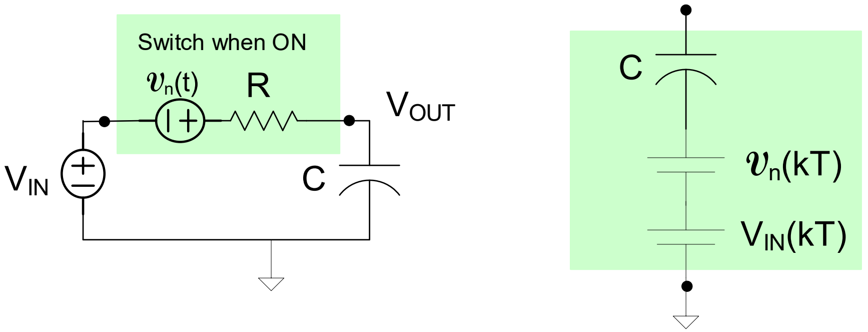
$$S_{V_n} = 4kTR$$

- Will show that noise due to switches sampling on a simple capacitor look like "capacitive" noise

$$V_{RMS} = \sqrt{\frac{kT}{C}}$$

Noise in switched capacitor circuits

Consider a capacitor that is sampling an input signal V_{IN}



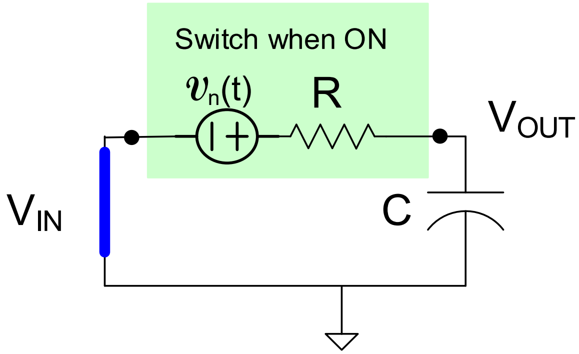
Track mode

Hold mode
(ideally)

Neither the noise voltage nor the input voltage sampled onto C will be ideal if R is not near 0Ω because of delay in the RC circuit

Noise in Basic Capacitive Sampler

During sampling phase



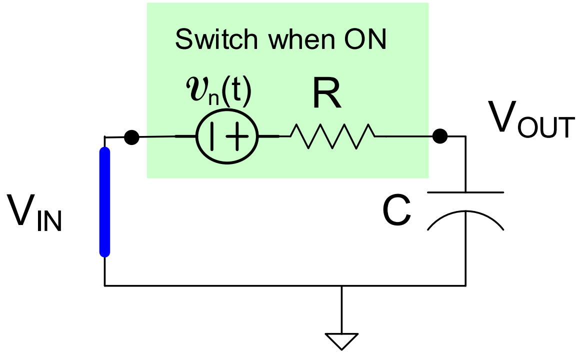
$$S(\omega) = S_{IN}\left|T(j\omega)\right|^2$$

$$T(s) = \frac{1}{1+RCs}$$

$$S_{Vn} = 4kTR$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

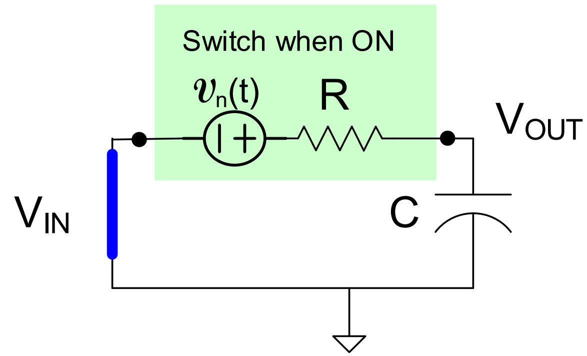
Noise during sampling phase



$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,df}$$

Noise during sampling phase

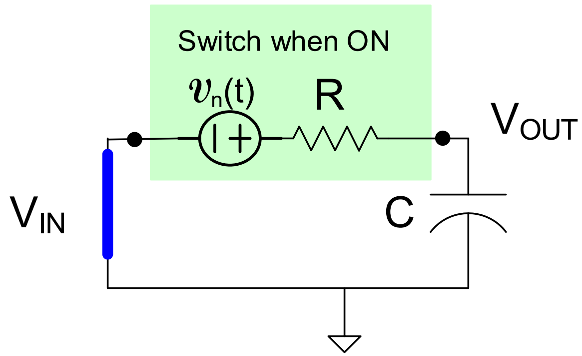


$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2 R^2 C^2}\, df}$$

It can be shown that this integral is independent of R and is given by

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$

Noise during sampling phase



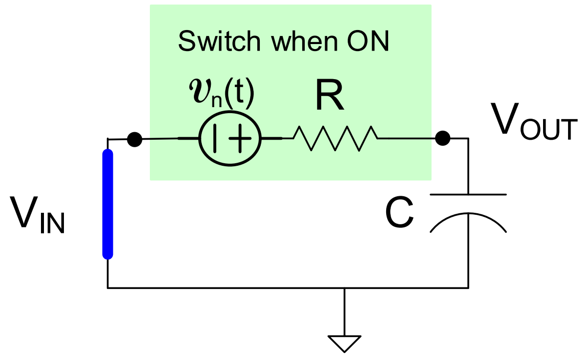
$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

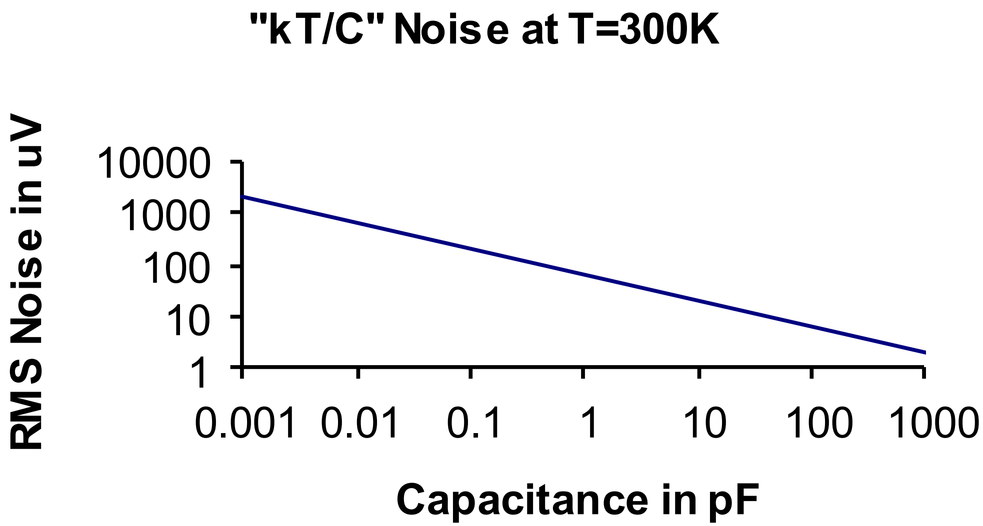
RMS noise voltage on C is independent of the state of the switch as long as it is ON

So sampled RMS noise voltage should be same as instantaneous RMS voltage

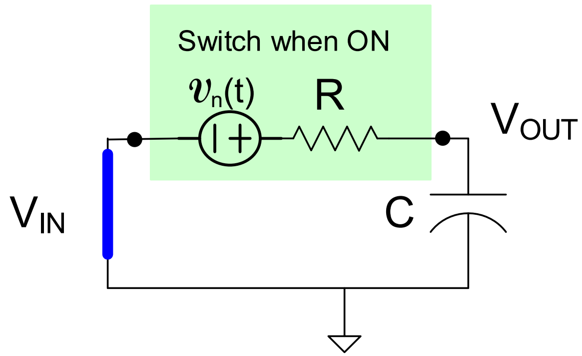
Highly temperature dependent

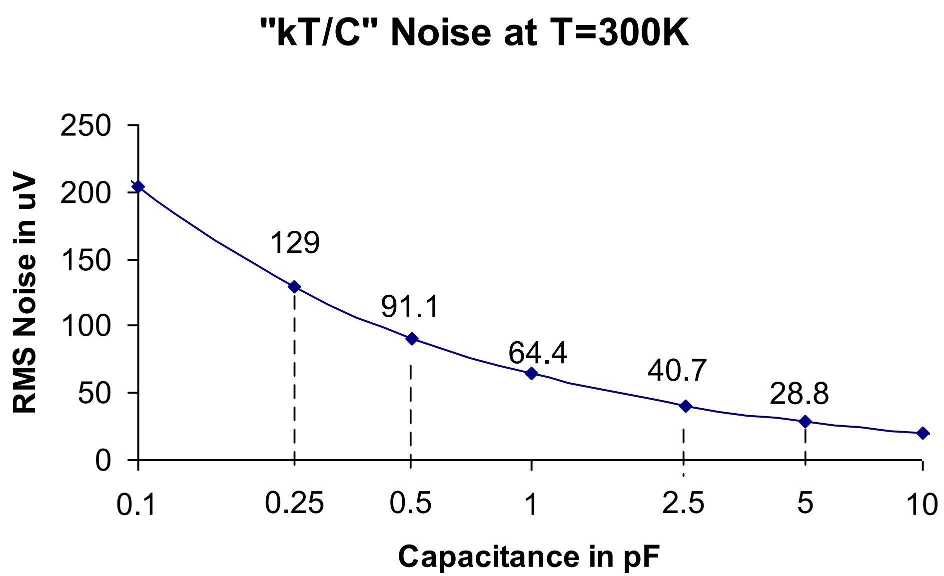
Noise during sampling phase





Noise during sampling phase





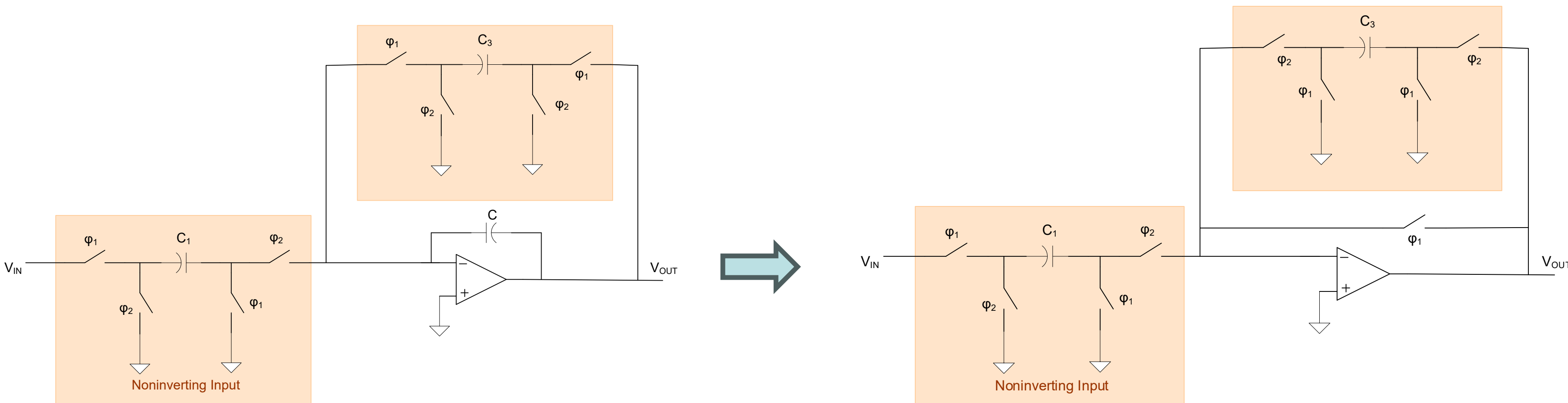
Noise in Simple Switched-Capacitor Sampler

- Capacitors do not have any noise source
- Switches contribute thermal noise
- Noise due to switches looks like "capacitive" noise $V_{RMS} = \sqrt{\frac{kT}{C}}$

Be careful with calculating noise in SC circuits !

Switched Capacitor Amplifiers

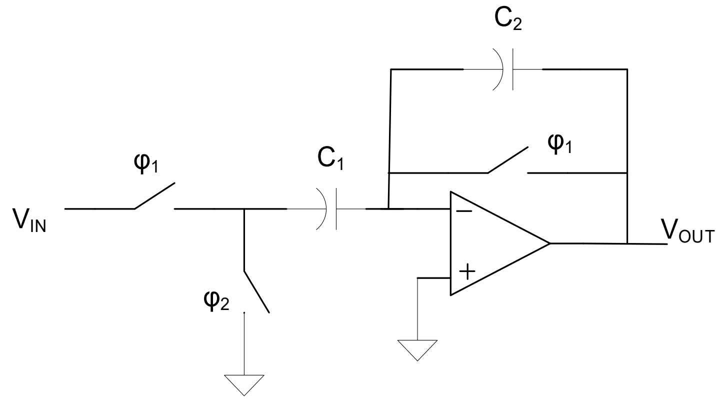
Elimination of the Integration Capacitor

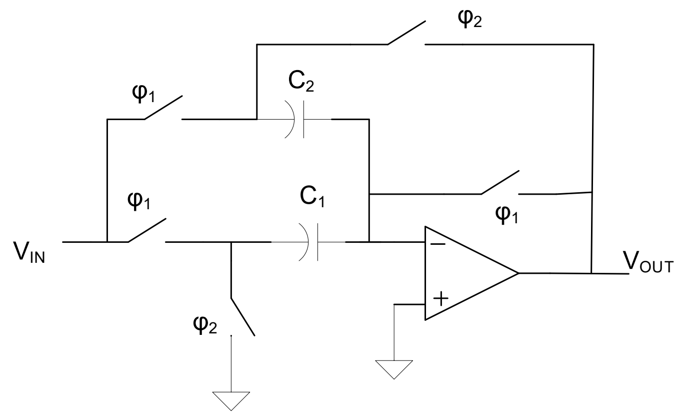


What happens if the integration capacitor is eliminated?

- Serves as a SC amplifier with gain of $A_V=C_1/C_2$
- Output is only valid during phase φ_2
- Summing inputs can be easily added
- SC amplifiers and SC summing amplifiers are widely used in filter and non-filter applications

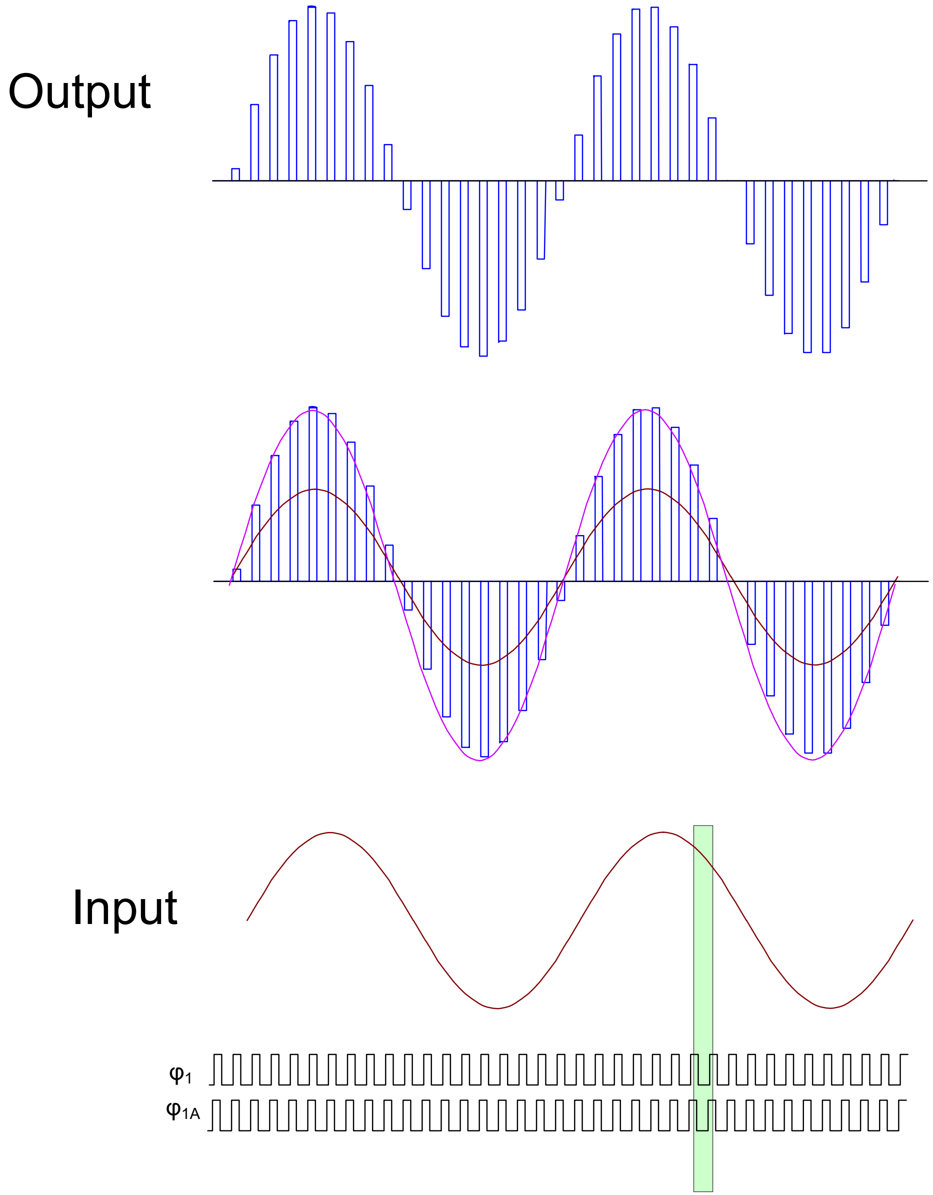
Switched Capacitor Amplifiers

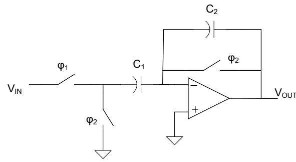




- Summing, Differencing, Inverting, and Noninverting SC Amplifiers Widely Used
- Significant reduction in switches from what we started with by eliminating C in SC integrator
- Must be stray insensitive in most applications
- Outputs valid only during one phase

Switched Capacitor Amplifiers





Voltage Mode Integrators

- Active RC (Feedback-based)
- MOSFET-C (Feedback-based)
- OTA-C
- TA-C

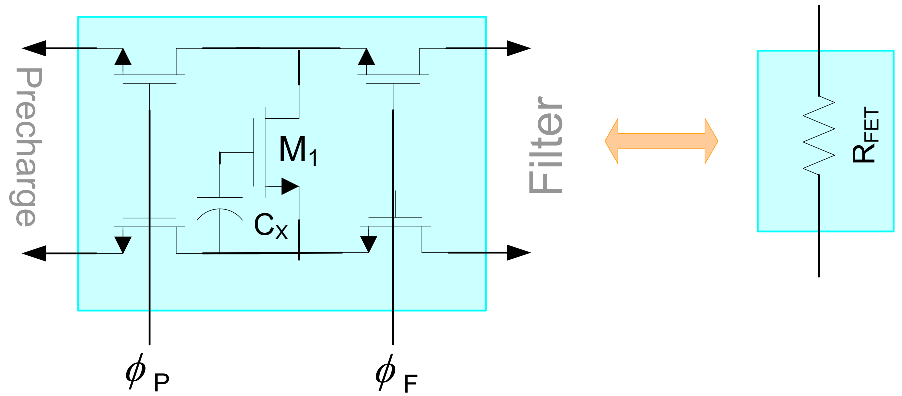
Sometimes termed "current mode"

- Switched Capacitor
- Switched Resistor

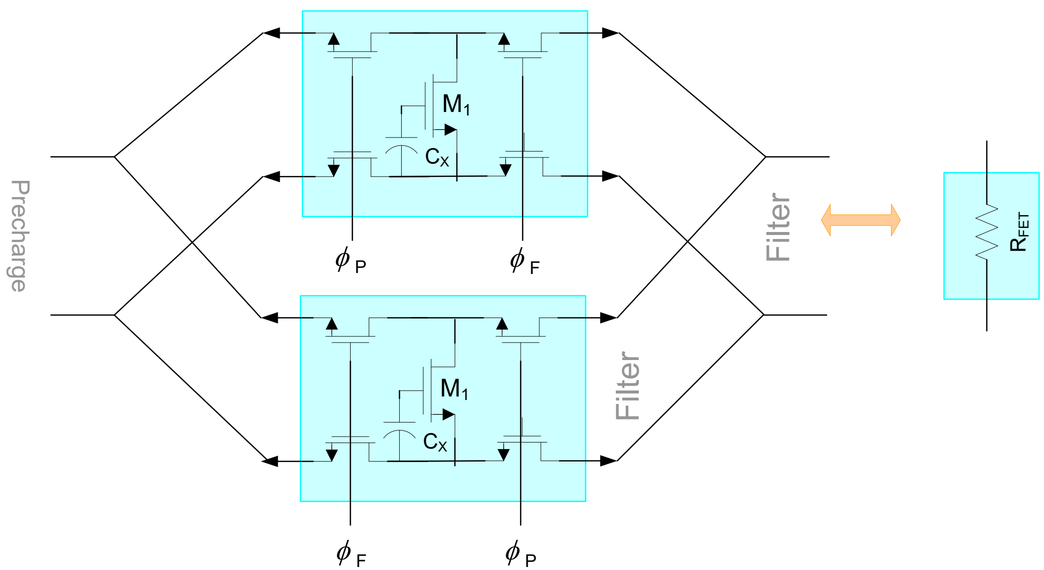
Will discuss later

- Other Structures

Switched-Resistor Voltage Mode Integrators



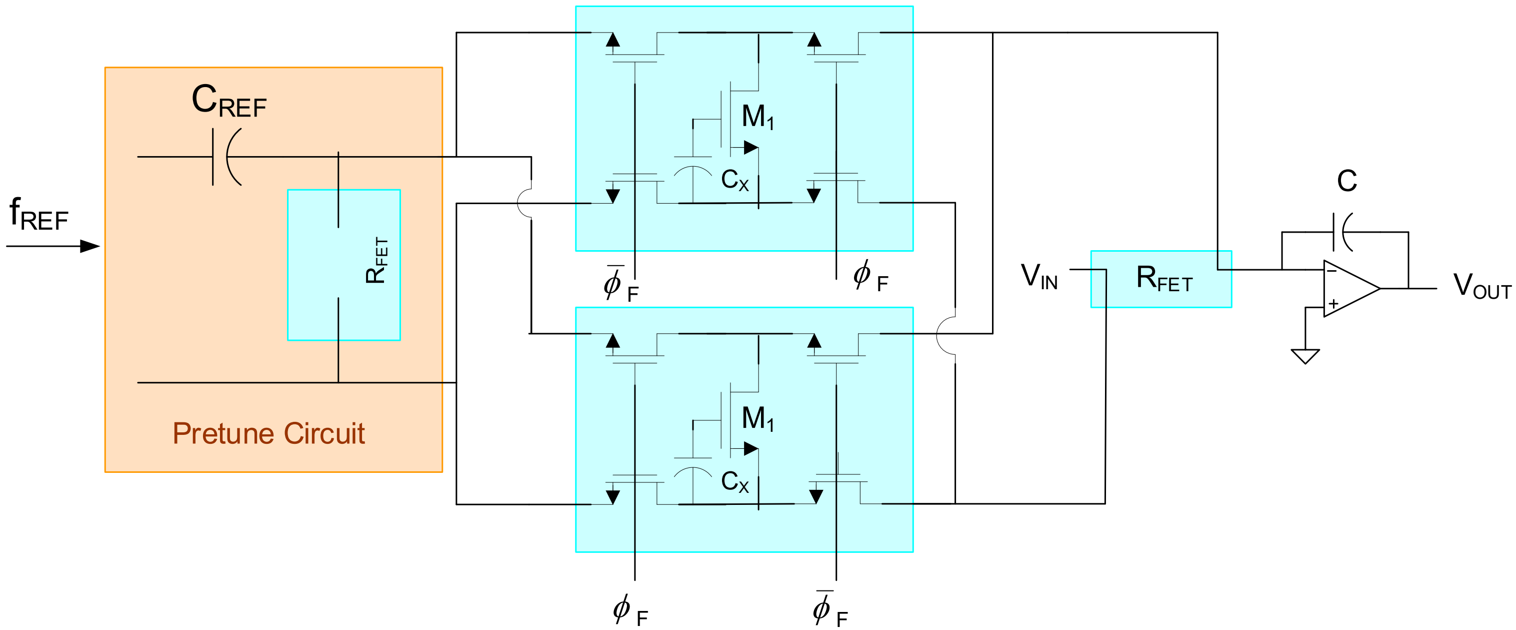
Observe that if a triode-region MOS device is switched between a precharge circuit and a filter circuit (or integrator) and V_{GS} is held constant, It will behave as a resistor while in the filter circuit



$$R_{FET} \cong \frac{L}{\mu C_{OX} W \left(V_{GS} - V_T\right)}$$

Observe that if two such circuits are switched between a precharge circuit and a filter circuit (or integrator) and V_{GS} is held constant, it will behave as a resistor in the filter circuit at all times

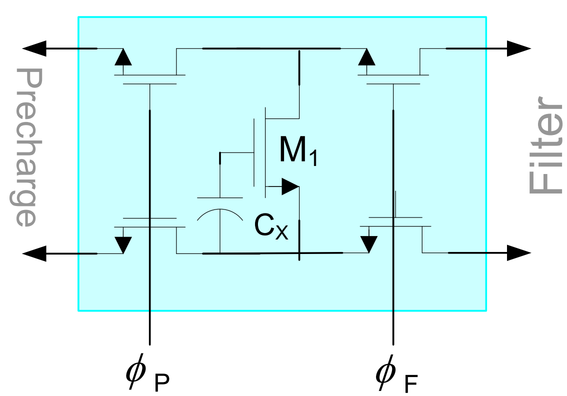
Switched-Resistor Voltage Mode Integrators

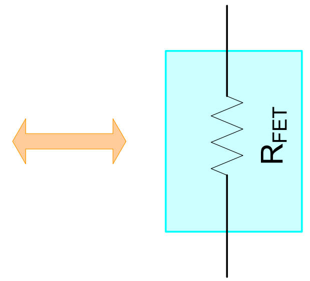


Switched-resistor integrator

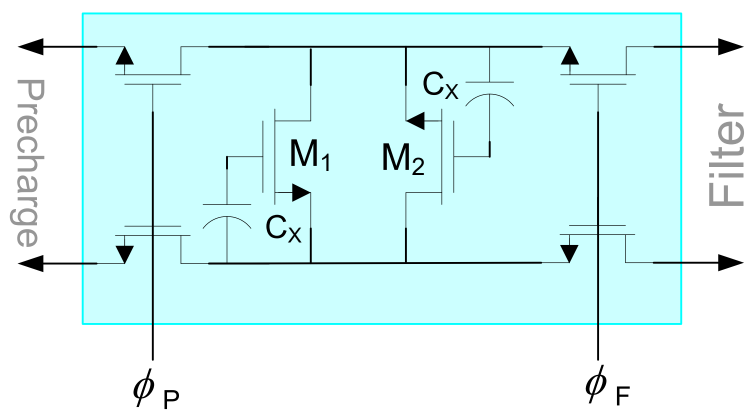
- Clock frequency need only be fast enough to prevent droop on C_X
- Minor overlap or non-overlap of clock plays minimal role in integrator performance
- Switched-resistors can be used for integrator resistor or to replace all resistors in any filter
- Pretune circuit can accurately establish $R_{FET}C_{REF}$ product proportional to f_{REF}
- $R_{FET}C$ product is given by $R_{FET}C = R_{FET}C\frac{C_{REF}}{C_{REF}} = [R_{FET}C_{REF}]\bullet\left[\frac{C}{C_{REF}}\right]$ and is thus accurately controlled

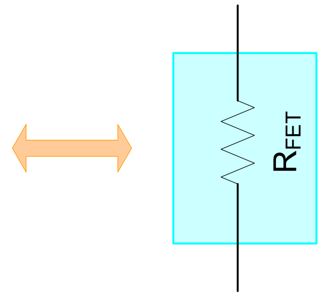
Switched-Resistor Voltage Mode Integrators





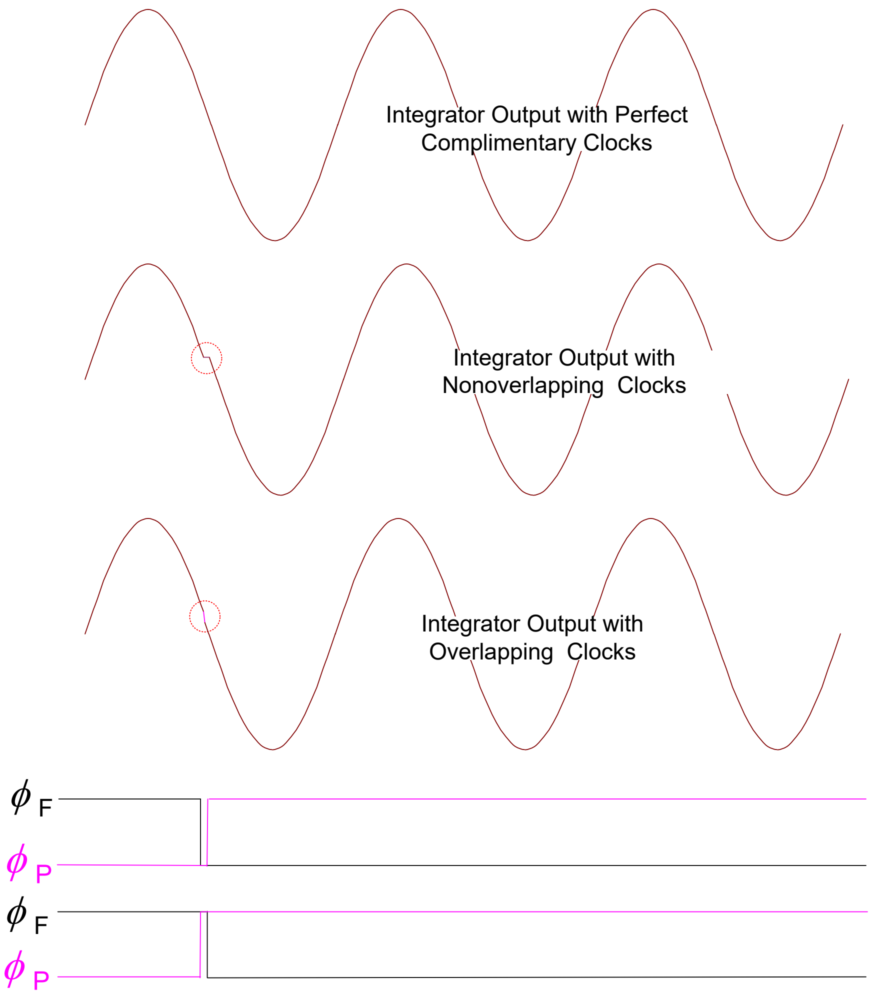
There are some modest nonlinearities in this MOSFET when operating in the triode region





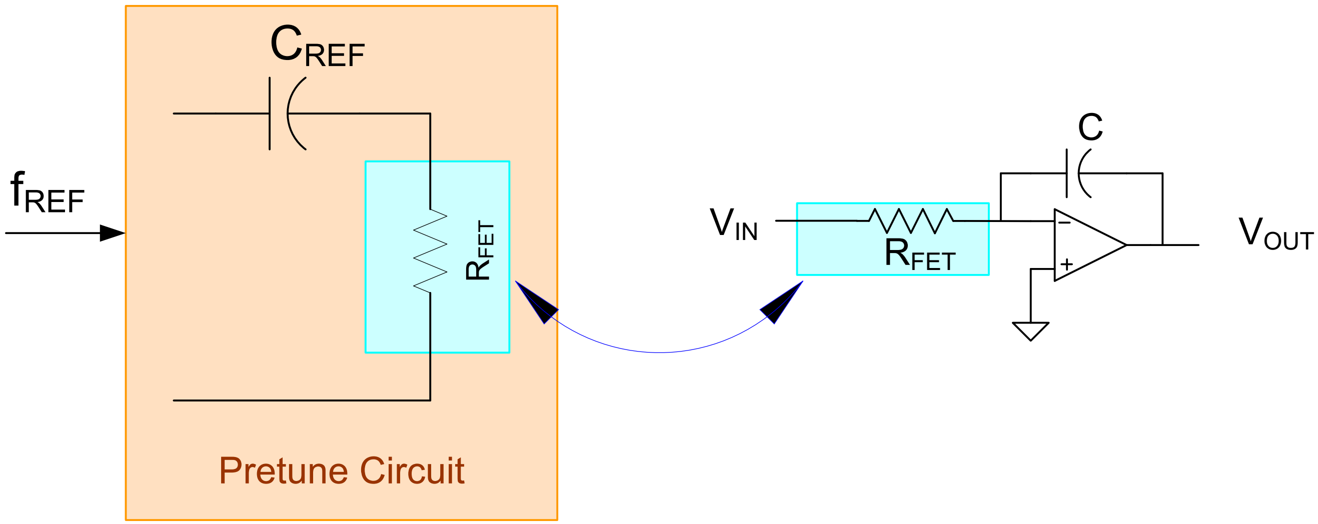
- Significant improvement in linearity by cross-coupling a pair of triode region resistors
- Perfectly cancels nonlinearities if square law model is valid for M_1 and M_2
- Only modest additional complexity in the Precharge circuit

Switched-Resistor Voltage Mode Integrators



- Aberrations are very small, occur very infrequently, and are further filtered
- Play almost no role on performance of integrator or filter

Switched-Resistor Voltage Mode Integrators



Switched-resistor integrator

- Accurate CR_{FET} products is possible
- Area reduced compared to Active RC structure because R_{FET} small
- Single pretune circuit can be used to “calibrate” large number of resistors
- Clock frequency not fast and not critical (but accuracy of f_{REF} is important)
- Since resistors are memoryless elements, no transients associated with switching
- Since filter is a feedback structure, speed limited by BW of op amp

Voltage Mode Integrators

- Active RC (Feedback-based)
- MOSFET-C (Feedback-based)
- OTA-C
- TA-C

Sometimes termed "current mode"

- Switched Capacitor (Feedback-based)
- Switched Resistor (Feedback-based)

Discrete Time

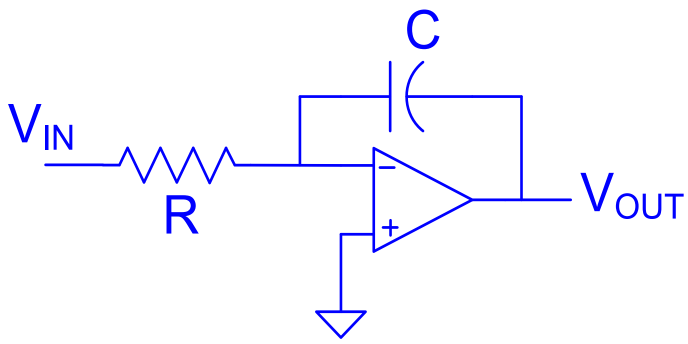
- Other Structures

Have introduced a basic voltage-mode integrators in each of these approaches

All of these structures have applications where they are useful

Performance of feedback-based structures limited by Op Amp BW

Variants of basic inverting integrator have been considered



Basic Miller Integrator

- Active RC
- MOSFET-C
- OTA-C
- g_m-C
- Switched-Capacitor
- Switched-Resistor

Performance of all is limited by GB of Operational Amplifiers

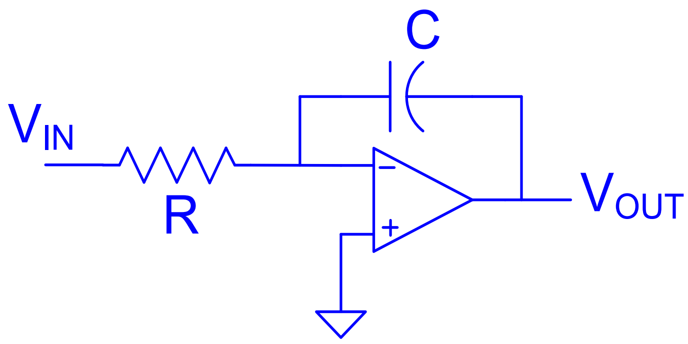
How can integrator performance be improved?

- Better op amps
- Better Integrator Architectures

How can the performance of integrator structures be compared?

Need metric for comparing integrator performance

Variants of basic inverting integrator have been considered



Basic Miller Integrator

- Active RC
- MOSFET-C
- OTA-C
- g_m-C
- Switched-Capacitor
- Switched-Resistor

Performance of all is limited by GB of Operational Amplifiers

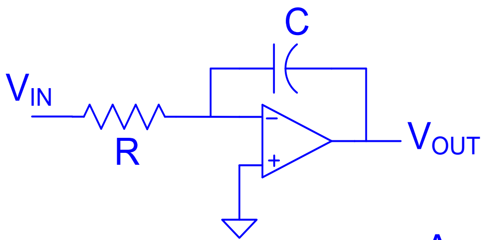
Consider Active RC class

Are there Other Integrators in this Class?

And, if so, how does their performance compare?

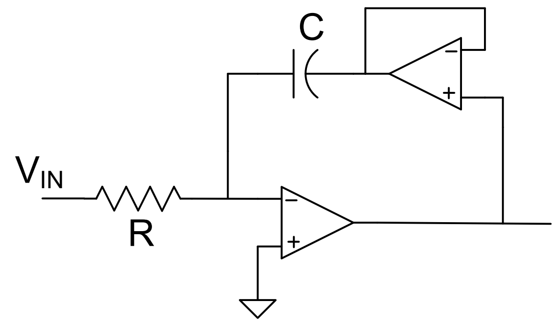
Are there other integrators in the basic classes that have been considered?

Consider Active RC class



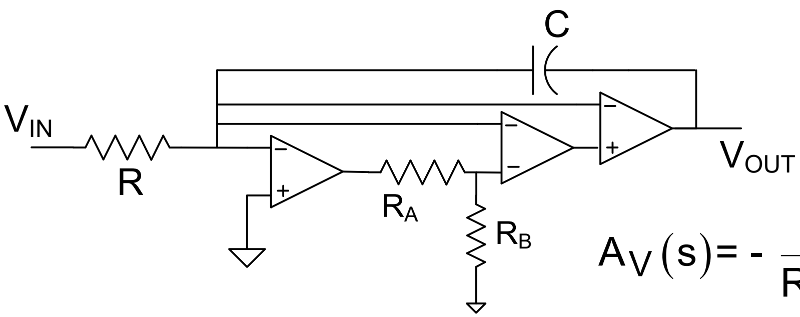
$$A_V(s) = -\frac{1}{RCs}$$

Miller Inverting



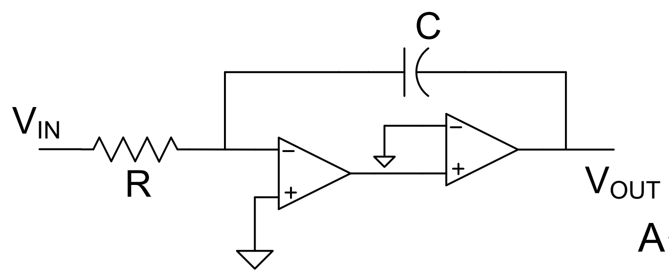
$$A_V(s) = -\frac{1}{RCs}$$

High-Q Inverting



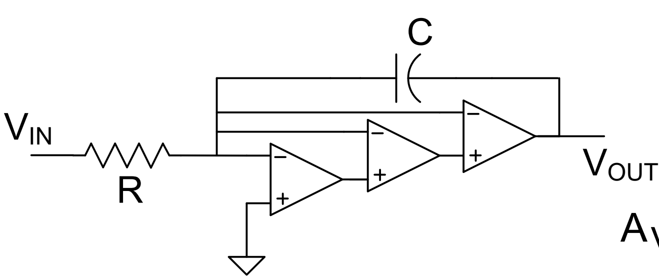
$$A_V(s) = -\frac{1}{RCs}$$

Zero Second Derivative Inverting



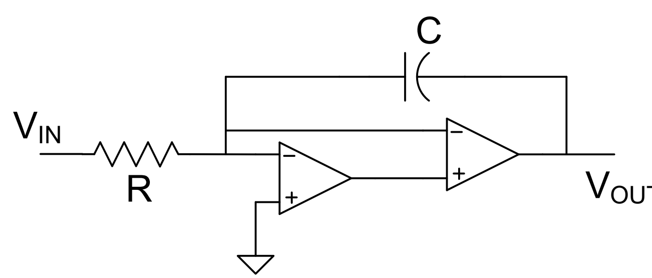
$$A_V(s) = -\frac{1}{RCs}$$

Cascaded Inverting



$$A_V(s) = -\frac{1}{RCs}$$

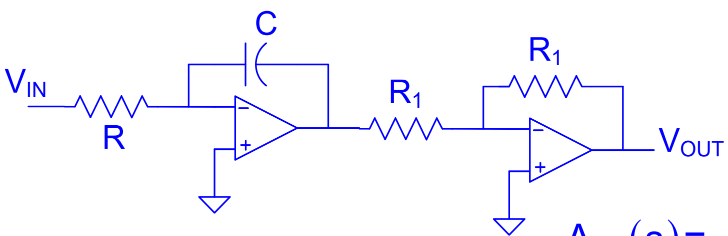
Zero Second Derivative Inverting



$$A_V(s) = -\frac{1}{RCs}$$

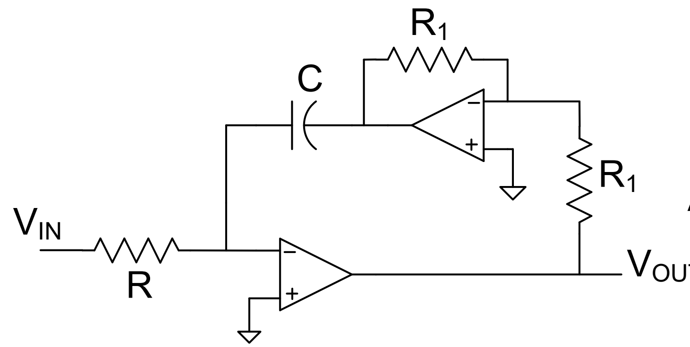
Zero Sensitivity Inverting

Are there other integrators in the basic classes that have been considered?



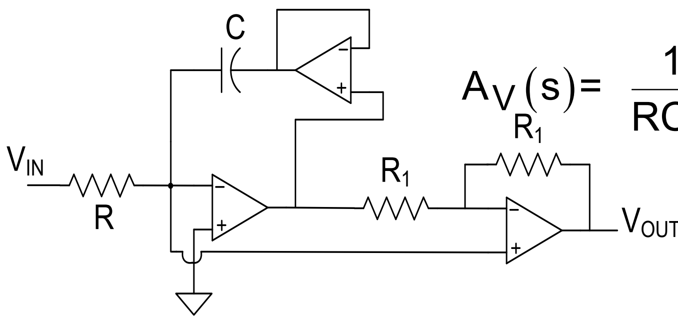
Miller Noninverting

$$A_V(s)=\frac{1}{RCs}$$



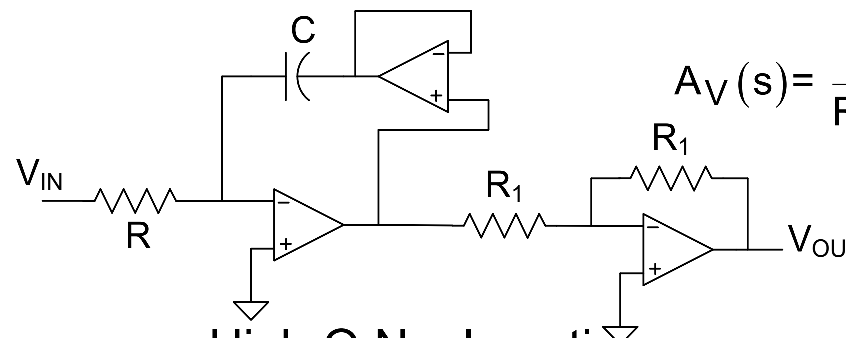
$$A_V(s)=\frac{1}{RCs}$$

Phase Lead Integrator



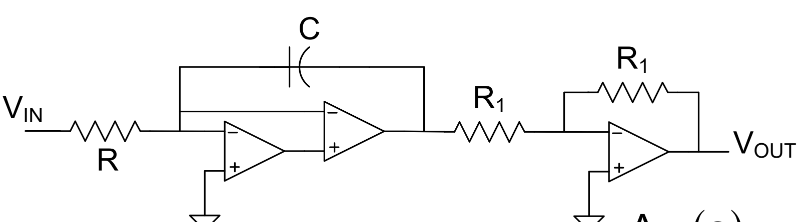
$$A_V(s)=\frac{1}{RCs}$$

Modified High-Q Noninverting



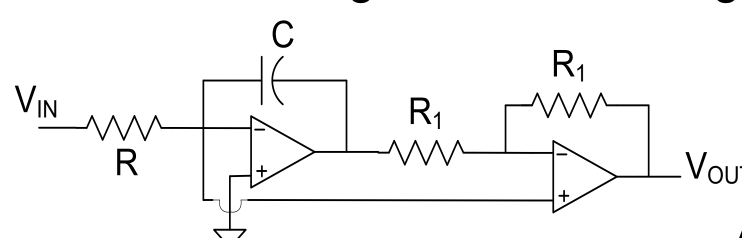
$$A_V(s)=\frac{1}{RCs}$$

High-Q NonInverting



$$A_V(s)=\frac{1}{RCs}$$

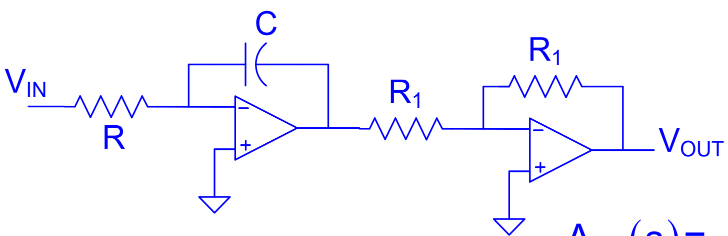
Zero Sensitivity Noninverting



$$A_V(s)=\frac{1}{RCs}$$

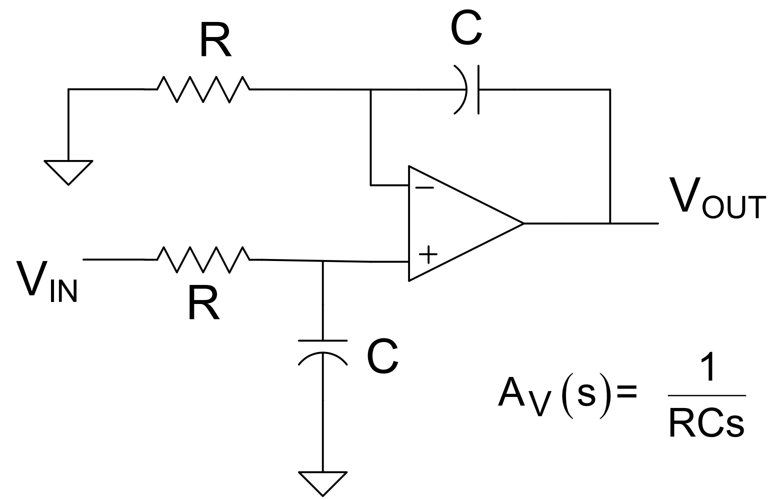
Modified Miller Noninverting

Are there other integrators in the basic classes that have been considered?



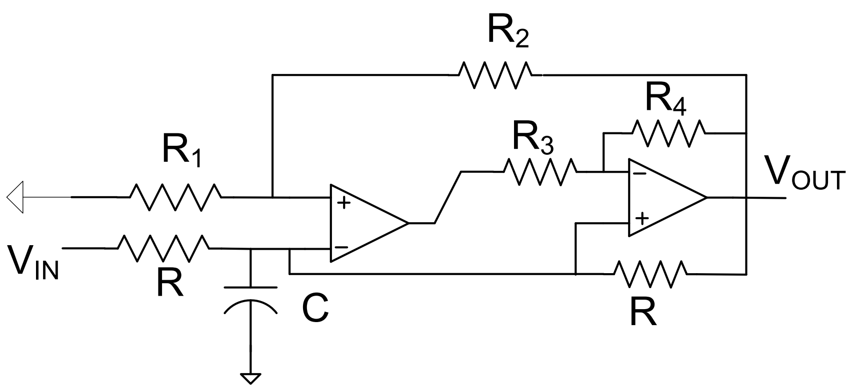
Miller Noninverting

$$A_V(s) = \frac{1}{RCs}$$



$$A_V(s) = \frac{1}{RCs}$$

Balanced Time Constant Noninverting



Zero Sensitivity Noninverting

$$A_V(s) = \frac{2}{RCs}$$

If $R_1=R_2$ and $R_3=R_4$

(note this has a grounded integrating capacitor!)

Stay Safe and Stay Healthy !

End of Lecture 29